UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/389,491	09/03/99	LEE K	028213-0101

MMC2/0228

KILE MCINTYRE, HARBIN & LEE
1101 PENNSYVANIA AVENUE N.W
SUITE 800REET NW
WASHINGTON DC 20004

EXAMINER	
BROCK II,P	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 02/28/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/389,491	LEE ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *1-11 and 25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-24 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Claims 1 - 11 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

Upon reviewing the elected claims drawn to the Group II method of making claims, claim 25 should have been grouped with the Group I device claims. Claim 25, therefore, is hereby withdrawn from consideration consistent with the applicant's election.

2. Applicant's election without traverse of Group II claims 12 – 24 and 26 in Paper No. 5 is acknowledged.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 20 and 22 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for the elements in (i) and (ii), does not reasonably provide enablement for (iii). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. There is no disclosure regarding the composition or proportion of the combination of elements from (i) and (ii) covered by the phrase "mixtures thereof".

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 12 – 16, 18 – 22, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gambino et al. in view of Hayden.

Gambino et al. discloses a method of making a semiconductor integrated circuit capacitor in figures 11 – 26.

With regard to claim 12, Gambino et al. discloses in figure 11 providing an insulating substrate (305). Gambino et al. discloses in figure 11 simultaneously forming a first wire line (315) and a lower electrode (310) on predetermined surfaces of the insulating substrate. Gambino et al. discloses in figure 11 forming an interlevel insulating layer (307) on the substrate, on the first wire line, and on the lower electrode. Gambino et al. discloses in figure 12 selectively etching the interlevel insulating layer to expose a predetermined surface of the lower electrode and a predetermined surface of the first wire line thereby simultaneously forming in the interlevel insulating layer: (i) a first via hole (320) having sidewalls and disposed above the lower electrode; and (ii) a second via hole (330) disposed above the first wire line. Gambino et al. discloses in figure 13 forming a conductive layer (328) on the interlevel insulating layer and in the first and second via holes. Gambino et al. discloses in figure 14 etching back the conductive layer to form: (ii) a conductive plug in the second via hole; and (iii) an exposed surface containing the conductive plug, the predetermined surface of the lower electrode, and

predetermined surfaces of the interlevel insulating layer. Gambino et al discloses in figure 15 forming a dielectric layer on the exposed surface. Gambino et al. discloses in figure 16 removing (332 and 334) the dielectric layer on the exposed surface except for a predetermined portion of the dielectric layer disposed on a predetermined surface of the lower electrode. Gambino discloses in figures 17 – 18 simultaneously forming: (i) a second wire line (324) connected to the conductive plug; and (ii) an upper electrode (324) connected to the dielectric layer. Gambino et al. does not disclose etching back the conductive layer to form: (i) a spacer on the sidewalls of the first via hole. Hayden teaches in figure 4 etching back a conductive layer to form: (i) a spacer (32) on the sidewalls of a first via hole (30). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the conductive spacers of Hayden in the first via hole of Gambino et al. in order to maximize the area of the capacitor as stated by Hayden in column 4, lines 28 – 30. Once the conductive spacers were formed in the first via hole of Gambino et al. it is obvious that the exposed surface would contain the spacer, and the dielectric layer would remain disposed on a predetermined portion of the spacer.

With regard to claim 13, Hayden et al teaches in column 4, line 20 the spacer is made from a conductive layer comprising a tungsten containing material.

With regard to claim 14, Gambino et al. discloses in column 5, line 33 that the dielectric layer has a structure a single-level structure containing an oxide layer or a nitride layer.

With regard to claim 15, Gambino et al. discloses in column 8, lines 7 –11 the oxide layer is made using a deposition technique employing Plasma Enhanced Oxide (PEOX). It is inherent that PECVD as described in line 17 is the same as PEOX when depositing oxide.

With regard to claim 16, Gambino et al. discloses in column 6, lines 13 – 17 the nitride layer is made using a deposition technique employing Plasma Enhanced Nitride (PESiN). It is inherent that PECVD as described in line 17 is the same as PESiN when depositing nitride.

With regard to claim 18, Gambino et al. discloses in column 5, lines 31 – 45 the lower and upper electrodes are made of aluminum. It is inherent that aluminum used in the processing of silicon wafers is an alloy of aluminum and silicon.

With regard to claim 19, Gambino et al. discloses in column 5, lines 37 – 39 an anti-reflection layer is disposed on the lower and/or upper electrode's surface.

With regard to claim 20, Gambino et al. discloses I column 5, lines 37 – 39 wherein the anti-reflection layer has a single level structure comprised of Ti.

With regard to claim 21, Gambino et al. discloses in column 5, lines 37 – 39 a barrier layer is disposed on the lower and/or upper electrode's surface.

With regard to claim 22, Gambino et al. discloses in column 5, lines 37 – 39 wherein the barrier layer has a single level structure comprised of Ti.

With regard to claim 24, Gambino et al. discloses in column 7, lines 39 – 48 the interlevel insulating layer is selectively etched by the process of dry etching. Reactive ion etching, as disclosed in column 7, line 48 is a dry etching process.

With regard to claim 26, Hayden teaches in figure 4 the spacer formed on the sidewalls of the via hole has a sloping surface.

7. Claims 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gambino et al., and Hayden as applied to claim 12 above, and further in view of Oh et al.

Gambino et al. discloses in column 5, line 33 that the dielectric layer has a single-level structure containing an oxide layer or a nitride layer. Gambino et al. and Hayden do not disclose that the dielectric layer has a multi-level structure containing layers selected from the group consisting of oxide layers, nitride layers, and mixtures thereof. Oh et al. teaches in column 4, lines 49 – 51 a dielectric layer that has a structure selected from: (i) a single-level structure containing an oxide layer or nitride layer; or (ii) a multi-level structure containing layers selected from the group consisting of oxide layers, nitride layers and mixtures thereof. Oh et al. teaches the multi-level structure is an oxide/nitride/oxide layer (ONO). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the ONO layer of Oh et al. in the process of Gambino et al, and Hayden in order to form a capacitor dielectric material as is well known in the art.

8. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gambino et al. and Hayden as applied to claim 12 above, and further in view of Nulty et al.

Gambino et al. and Hayden do not disclose further comprising, after forming the first and second via holes, RF sputter etching the interlevel insulating layer and the first and second via holes. Nulty et al. teaches in column 2, lines 56 – 60 RF sputter etching an interlevel insulating layer and via holes. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the RF sputter etching of Nulty et al. in the process of Gambino et al and Hayden in order to remove native oxide on top of the conducting layers as stated by Nulty et al. in column 2, lines 56 – 60.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yasunari, and Wang et al. disclose forming multiple vias on an insulative semiconductor substrate. An et al. and Saenger et al. disclose forming conductive spacers for capacitors. Strahl discloses an RF sputter etching for removal of native oxides. Worley et al. discloses the use of a layered dielectric material for capacitors consisting of layers of oxide and nitride.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
February 7, 2001

EDDIE C. LEE
PRIMARY EXAMINER